Electronic Version
Stylesheet Version v1.1.1

ACCURATE TIMING ANALYSIS OF INTEGRATED CIRCUITS WHEN COMBINATORIAL LOGIC OFFERS A LOAD

Abstract

The accuracy of timing analysis of an integrated circuit is enhanced based on an observation that the capacitive load offered by a combinatorial element (e.g., logic gate) is more when the value on the output path switches, compared to in a scenario when the output path does not switch. In an embodiment, the capacitance value corresponding to the case of switching is associated with cells if setup time violations are of concern, and the capacitance value corresponding to the non-switching case is associated with cells (libraries) if hold time violations are of concern.